InGaAs finFETs for future CMOS

Regardless of its form, the silicon transistor is tipped to offer diminishing returns at the 7 nm CMOS node and beyond.

Can the InGaAs finFET step in and maintain the march of Moore's Law?

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The last few years have witnessed an explosion of interest in exploring the use of III-Vs to advance logic CMOS beyond the point of diminishing returns for silicon technology. There is now a tantalizing possibility that these compound semiconductors will enter the CMOS roadmap. If they do, the benefits could be huge – they could extend Moore's Law by two or three more nodes, a huge contribution in itself, and they could also hold the key to revolutionary new technologies that are enabled by the integration of III-Vs on silicon. This combination could create systems that combine logic, terahertz sensing, imaging and communications, as well as optical functions.

When it comes to prototyping III-V based transistors for silicon integration, InGaAs is attracting the most attention. Its greatest virtue is its outstanding electron velocity that has enabled the fabrication of record-breaking HEMTs and HBTs. But interest in this ternary goes beyond its high speed credentials. By adjusting its composition, InGaAs can span a wide range of lattice constants, effective masses and bandgaps.

This allows the fine-tuning of its electrical properties. What's more, this alloy can be paired with other III-Vs, such as InAlAs and InP, to provide the possibility for flexible, powerful, bandgap and strain engineering. InGaAs also has the merit of forming oxide-semiconductor interfaces of excellent quality when partnered with a high-*k* dielectric.

Armed with all these attributes, InGaAs has recently been used to form planar MOSFETs with impressive characteristics. Their fabrication, which has fuelled further confidence in the potential of this material system, has drawn on the development of highly scaled MOS gate stacks with excellent interfacial characteristics, ohmic contacts with low contact resistance, and very tight self-aligned designs.

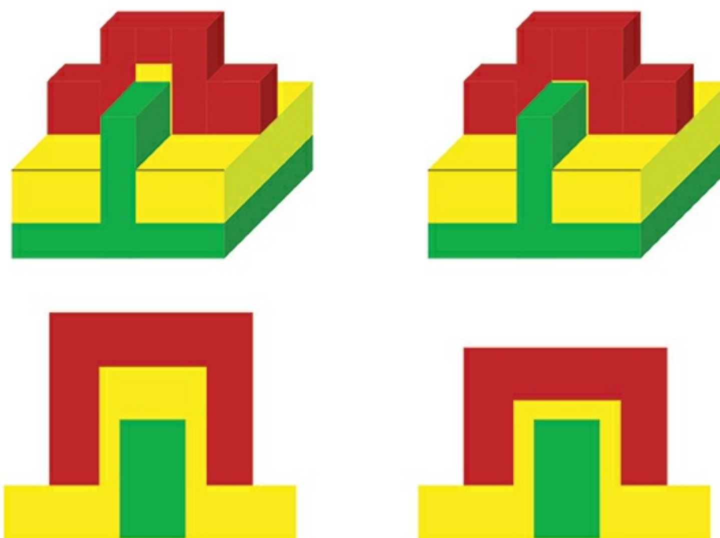

Figure 1. Two breeds of finFETs: a double-gate MOSFET and a trigate MOSFET.

While the planar InGaAs MOSFET has been an excellent platform for exploring process development and device physics, its scaling potential is limited – gate lengths below 40 nm do not seem feasible. That is not a major concern, though, as three-dimensional transistor structures, such as finFETs, trigate FETs, or nanowire MOSFETs, will be needed at the most likely point of insertion into the CMOS roadmap. Only these architectures can attain the footprint that will comply with Moore's Law transistor density goals.

As its name suggests, the conducting channel in a finFET resides in a thin 'fin' of semiconductor that sticks out of the wafer surface. With this architecture, the transistor gate can either be placed on two sides to create a double-gate MOSFET, or on three to form a trigate MOSFET. Both geometries yield a high degree of electrostatic control, enabling scaling of the gate length to very small dimensions (see Figure 1). Of the two, it is the trigate structure that is used today in state-of-the-art silicon MOSFETs in the most advanced CMOS nodes.

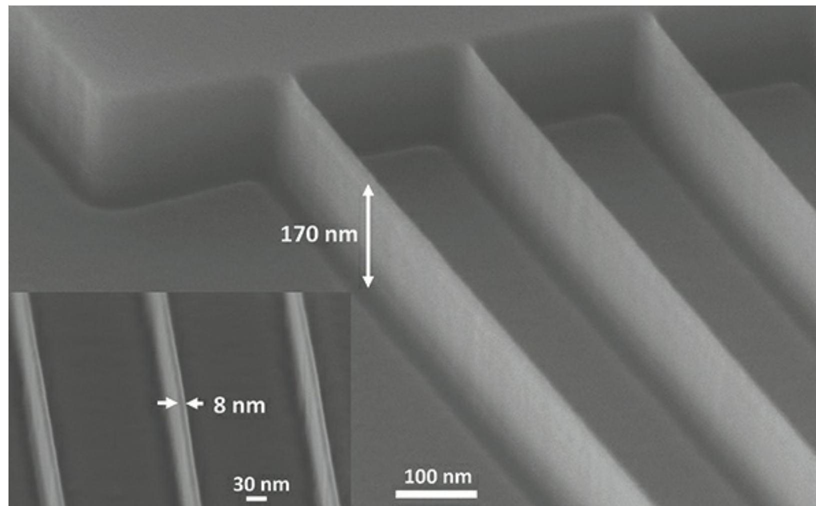

Figure 2. InGaAs fin array etched by reactive ion etching followed by three cycles of digital etch. The final fin width is 8 nm and the fin height is 170 nm (aspect ratio = 21).

During the last few years, several groups have demonstrated finFETs with an InGaAs channel. Unlike planar InGaAs MOSFETs, performance is rather unimpressive, due to challenges that are unique to finFETs and yet to be tackled. At MIT we are working on these issues, and have made significant strides, with successes including an etching process that can yield high-quality, vertical fins and a novel approach for adding metal contacts. The devices that result are setting a new benchmark for this class of transistor, when judged in terms of key metrics.

InGaAs fins

With the finFET, device performance depends a great deal on the quality of the fin. At the point of insertion into the CMOS roadmap, transistors must sport a fin width of less than 10 nm and an aspect ratio in excess of 5 – in other words, the channel must be at least five times as high as it is wide.

To produce fins with this geometry, several teams have pursued bottom-up techniques based on aspect-ratio trapping. This approach, which involves the growth of compound semiconductor heterostructures in a narrow dielectric trench, is attractive because it enables relatively straightforward integration of III-Vs on a silicon wafer. Dislocations arising from lattice mismatch between silicon and the III-V heterostructure are annihilated at the sidewalls, leading to defect-free material towards the top of the fin. Well, that's the promise. In practice, however, the fin contains residual defects and atomic intermixing, resulting in poor transistor isolation and bad performance.

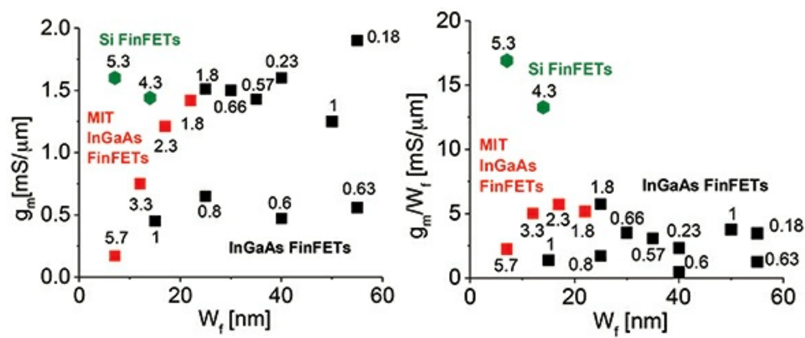

Figure 3. Benchmark of transconductance of InGaAs finFETs. Left: Transconductance normalized by conducting gate periphery. Right: Transconductance normalized by fin width. State-of-the-art silicon finFETs are included for reference. The red squares are recent results from MIT.

Approaching the challenge from the opposite direction are top-down techniques. They include reactive ion etching, a process that can yield high-aspect-ratio fins with vertical sidewalls.

We have refined this technique, using a combination of BCl_3, $SiCl_4$ and argon to etch III-Vs and form fins. We have also demonstrated trimming of the fin and smoothing of its sidewalls through so-called 'digital etch'. This highly controlled, self-limiting process preserves fin shape while smoothing the sidewalls. Combining our two techniques has enabled us to form InGaAs fins with a width of less than 10 nm and an aspect ratio in excess of 5 (see Figure 2).

With the finFET, the quality of the sidewall is critical. If it is excessively rough, or riddled with a loss of stoichiometry, the transistor can suffer from poor charge control and unsatisfactory transport characteristics.

To determine whether this could be the case in our devices, we have produced sidewall capacitors. These are special-purpose test structures that isolate the charge-control characteristics of the fin sidewalls. This investigation revealed that our digital etch process enhances the electrical quality of the sidewalls. Encouragingly, we also found that with proper treatment, the etched sidewall can produce a minimum interface state density on the order of 3×10^{12} eV^{-1} cm^{-2}. Although this is still on the high side of what is desirable, it is nevertheless a very promising result.

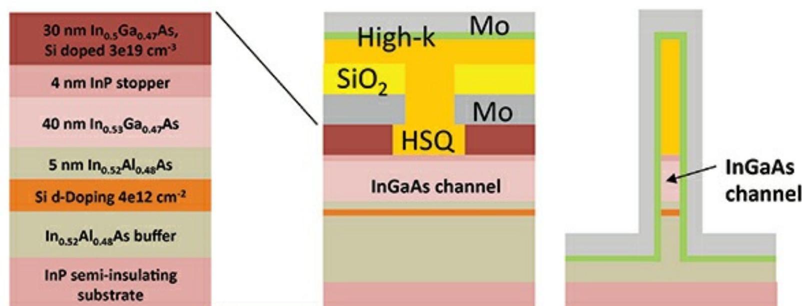

Figure 4. Longitudinal and transversal cross-sections of MIT's InGaAs finFETs.

Unfortunately, our study has uncovered an additional concern associated with the use of very thin etched InGaAs fins in finFETs. We found that the electron mobility rapidly degrades when the fin width drops below about 15 nm. We are still to perform a detailed study of this phenomenon, which should not raise eyebrows, given that similar observations have been made in highly scaled, ultra-thin-body silicon SOI-MOSFETs. Note that the implications of our finding may not be as severe as they initially appear, because at these length scales, the electron velocity has

far greater impact on device performance than electron mobility.

Producing a high-performance InGaAs finFET is not simply a matter of making a fin with a high aspect ratio and vertical, high-quality sidewalls. Additional features must include low-resistivity ohmic contacts, a tight self-aligned design and uniform, reproducible characteristics. Bringing all these elements together at the nanometre scale is very challenging, and an honest appraisal of the performance of today's InGaAs finFETs shows that there is still much work to do.

Benchmarking III-V finFETs

One key figure of merit for judging the performance of state-of-the-art transistors is transconductance. This characteristic, which reflects how quickly charge carriers move in the channel, is a critical metric in any transistor application.

We have benchmarked the transconductance of InGaAs finFETs with two different approaches: the conventional approach, which is to normalise transconductance by the conducting gate periphery; and an alternative method, where the same data is normalized by the fin width (see Figure 3). The latter approach makes a great deal of sense, because it relates to transistor density, which, in the end, is what Moore's Law is all about. Both graphs include estimations from selected state-of-the-art silicon finFETs (22 nm and 14 nm CMOS from Intel), along with our recently published results.

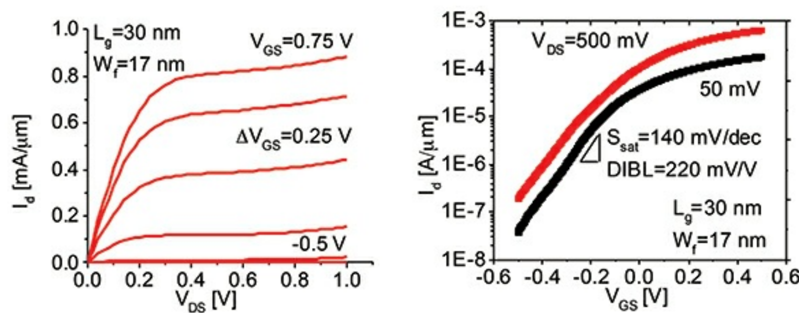

Figure 5. Output characteristics and sub-threshold characteristics of InGaAs finFET made at MIT (Wf=17 nm, Lg=30 nm)

Several interesting observations can be made from these graphs. First is the realization that while the latest generation of silicon finFETs already feature fins with a width of less than 10 nm and an aspect ratio in excess of 5, until our most recent results, the narrowest InGaAs finFETs presented in the literature had a fin width of 15 nm and an aspect ratio less than two. So, in reality, the vast majority of InGaAs finFETs are just barely so - in fact, they are almost planar devices! Our benchmarking also reveals that when normalized by conducting gate periphery, the transconductance of the best InGaAs finFETs are almost a match for silicon finFETs. This is in spite of the widely different aspect ratio, and the fact that planar InGaAs MOSFETs have demonstrated a very high transconductance – the current record, which is held by our group, is 3.45 mS/μm.

This discrepancy exposes a noteworthy difference between the silicon finFET and its InGaAs cousin. Sidewall charge control is successful in the silicon finFET, but in the InGaAs finFET it is far less effective. This is clear to see when transconductance is normalized by the fin footprint (see Figure 3 (b)). Normalising in this manner highlights the importance of extracting a lot of current drive out of a tiny transistor footprint, the essence of Moore's Law. When normalized in this way, the gap between silicon finFETs and InGaAs finFETs is clear, indicating that the development of the InGaAs finFET is in its infancy.

Included in the benchmarking data are our recent devices results, which we revealed earlier this summer at the

VLSI Technology Symposium. These devices have fin widths as narrow as 7 nm, aspect ratios in excess of 5, and gate lengths as short as 20 nm. Although these devices are inferior to state-of-the-art silicon finFETs, the transconductance, when normalized by fin width, is more than 50 percent higher than that of any other InGaAs finFET previously reported. So what is unique about these devices?

For starters, the design of our finFET breaks new ground. Its unique elements include ohmic contacts that are fabricated first, using low-resistivity molybdenum sputtered on the as-grown pristine surface. Our experience with planar InGaAs MOSFETs suggests that this approach yields record contact resistivities in the mid 0.1-1 $\Omega.\mu m^2$ range. Ultimately, values below 0.1 $\Omega.\mu m^2$ will be required.

The fins that we produce are formed by a combination of reactive-ion etching and digital etch. This yields smooth, highly vertical sidewalls. One feature of our process is that the reactive-ion etching mask used to define the fins is left in place. Consequently, after gate stack fabrication through atomic layer deposition of Al_2O_3 and HfO_2 and molybdenum gate sputtering and definition, the resulting device has a double-gate design. This means that the gate modulates only the electron concentration at the sidewalls, rather than also through the top, the situation that occurs in a trigate transistor.

This could be viewed as a deficiency, because the trigate design should provide better electrostatic control and current drive than the double-gate architecture. However, for very thin fins, the theoretical difference is very small. There are also significant upsides to our device geometry: the practical implementation of a trigate MOSFET is much harder, and it demands serious compromises in process and transistor design. Both take their toll, leading to increases in parasitic resistance, capacitance and leakage that impair transistor performance.

We have performed additional electrical characterisation of our finFETs, involving a device with 17 nm wide fins (see Figure 5). This shows that although our devices are record setting, they are still far from what can be accomplished with silicon. Clearly, a lot of work lies ahead of us.

Our research on highly scaled InGaAs finFETs reveals an additional issue of concern, which could impact future manufacturing. Due to strong quantum confinement in very thin fins, there is a steep dependence of the threshold voltage on fin width.

This behaviour, which stems from the very low electron effective mass in InGaAs, produces a positive shift in threshold voltage when fin widths decrease below 10 nm. The same trend occurs in silicon finFETs, but in InGaAs the sensitivity of threshold voltage to fin thickness is about four times higher. This greater sensitivity creates a great challenge for process control in a future manufacturing environment.

As we have shown, in the last few years, great progress has been made with the InGaAs finFET. Although its performance is inferior to that of state-of-the-art silicon transistors, that should not be too concerning, as the technology is still rather immature. Given the impressive strides made by planar InGaAs MOSFETs in recent times, there is good reason to believe that there is tremendous, pent-up potential with the InGaAs finFET.

Further reading

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